L Number	Hits	Search Text	DB	Time stamp
1	56308	(surface near5 (termination or terminate or terminating or modification or modify or modifying))	USPAT; US-PGPUB	2004/11/16 10:59
2	224	((surface near5 (termination or terminate or terminating or modification or modify or modifying))) and (ALD or (atomic adj layer adj deposition))	USPAT; US-PGPUB	2004/11/16 10:59
3	30	(((surface near5 (termination or terminate or terminating or modification or modify or modifying))) and (ALD or (atomic adj layer adj deposition))) and @ad<20001124	USPAT; US-PGPUB	2004/11/16 11:02
4	21	((((surface near5 (termination or terminate or terminating or modification or modify or modifying))) and (ALD or (atomic adj layer adj deposition))) and @ad<20001124) and plasma	USPAT; US-PGPUB	2004/11/16 11:02

US-PAT-NO: 6551399

DOCUMENT-IDENTIFIER: US 6551399 B1

TITLE: Fully integrated process for MIM capacitors using **atomic layer deposition**

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Abstract Text - ABTX (1):
A method and apparatus for fabricating a metal-insulator-metal capacitor by performing **atomic layer deposition (ALD)**. A fully integrated process flow prevents electrode-dielectric contamination during an essential ex situ bottom electrode patterning step.

TITLE - TI (1):
Fully integrated process for MIM capacitors using **atomic layer deposition**

Brief Summary Text - BSTX (3):
The present invention relates generally to semiconductor technology and, more particularly, to a method and apparatus for manufacturing metal-insulator-metal capacitors using **atomic layer deposition**.

Brief Summary Text - BSTX (6):
One variant of CVD to deposit thinner layers is a process known as **atomic layer deposition (ALD)**. **ALD** has its roots originally in atomic layer epitaxy, which is described in U.S. Pat. Nos. 4,058,430 and 4,413,022 and in an article titled "Atomic Layer Epitaxy" by Goodman et al., J. Appl. Phys. 60(3), Aug. 1, 1986; pp. R65-R80. Generally, **ALD** is a process

wherein conventional
CVD processes are divided into single-monolayer
depositions, wherein each
separate deposition step theoretically reaches saturation
at a single molecular
or atomic monolayer thickness and, then, self-terminates.

Brief Summary Text - BSTX (7):

The deposition is an outcome of chemical reactions
between reactive
molecular precursors and the substrate (either the base
substrate or layers
formed on the base substrate). The elements comprising the
film are delivered
as molecular precursors. The desired net reaction is to
deposit a pure film
and eliminate "extra" atoms (molecules) that comprise the
molecular precursors
(ligands). In a standard CVD process, the precursors are
fed simultaneously
into the reactor. In an **ALD** process, the precursors are
introduced into the
reactor separately, typically by alternating the flow, so
that only one
precursor at a time is introduced into the reactor. For
example, the first
precursor could be a metal precursor containing a metal
element M, which is
bonded to an atomic or molecular ligand L to form a
volatile molecule ML.sub.x.
The metal precursor reacts with the substrate to deposit a
monolayer of the
metal M with its passivating ligand. The chamber is purged
and, then, followed
by an introduction of a second precursor. The second
precursor is introduced
to restore the surface reactivity towards the metal
precursor for depositing
the next layer of metal. Thus, **ALD** allows for single layer
growth per cycle,
so that much tighter thickness controls can be exercised
over standard CVD
process. The tighter controls allow for ultrathin films to
be grown.

Brief Summary Text - BSTX (9):

Although currently manufactured MIM capacitors use CVD technology, none are known to have been fabricated by **ALD**. Since **ALD** has the ability to deposit continuous ultrathin films of conductive, semiconductive or insulating (dielectric) material on complicated geometries, yet retain good uniformity and conformity, **ALD** is attractive for fabricating MIM capacitors. The present invention is directed to providing the integration of **ALD** for the manufacture of MIM capacitors.

Brief Summary Text - BSTX (11):

A method and apparatus for depositing a first conductive layer by **atomic layer deposition** and depositing a sacrificial layer above the first conductive layer also by **atomic layer deposition** without exposing the first conductive layer to oxidation. A defined structure is then formed by removing portions of the first conductive and sacrificial layers. Next, the sacrificial layer is removed to expose the underlying first conductive layer without exposing the first conductive layer to oxidation. A dielectric layer is next deposited over the exposed first conductive layer by **atomic layer deposition**. To form a metal-insulator-metal (MIM) capacitor, the stack is completed by depositing a top conductive layer.

Drawing Description Text - DRTX (14):

FIG. 13 is a block diagram showing one reactor apparatus for performing **ALD,** as well as pretreating the surface of a layer prior to **ALD,** in order to fabricate an MIM capacitor practicing the present invention.

Detailed Description Text - DETX (2):

The practice of **atomic layer deposition (ALD)** to deposit

a film layer onto a
substrate, such as a semiconductor wafer, requires separately introducing
molecular precursors into a processing reactor. The **ALD** technique will deposit
an ultrathin film layer atop the substrate. The term substrate is used herein
to indicate either a base substrate or a material layer formed on a base
substrate, such as a silicon substrate. The growth of the **ALD** layer follows
the chemistries associated with chemical vapor deposition (CVD), but the
precursors are introduced separately.

Detailed Description Text - DETX (3):
In an example **ALD** process for practicing the present invention, the first
precursor introduced is a metal precursor comprising a metal element M bonded
to atomic or molecular ligand L to make a volatile molecule ML.sub.x (the x, y
and z subscripts are utilized herein to denote integers 1, 2, 3, etc.). It is
desirable that the ML.sub.x molecule bond with a ligand attached to the surface
of the substrate. An example ligand is a hydrogen-containing ligand, such as
AH, where A is a nonmetal element bonded to hydrogen. Thus, the desired
reaction is noted as AH+ML.sub.x.fwdarw.AML.sub.y +HL, where HL is the exchange
reaction by-product.

Detailed Description Text - DETX (4):
After the ML.sub.x precursor reacts with the **surface and self-saturates to terminate** the reaction, the remaining non-reacted precursor is removed,
typically by allowing the carrier gas to purge the processing chamber. The
second precursor is then introduced. Since the surface of the substrate
contains the MA--L combination, the second precursor reacts with the L
termination on the surface. In this example, the second

precursor is comprised
of AH.sub.z, with A being a nonmetal element. The hydrogen component is
typically represented by H.sub.2 O, NH.sub.3 or H.sub.2 S. The reaction
ML+AH.sub.z.fwdarw.MAH+HL results in the desired additional element A being
deposited as AH terminated sites and the ligand L is eliminated as a volatile
by-product HL. The surface now has AH terminated sites, which restore the
surface to have AH terminations. This restoration completes one **ALD** cycle, in
which a monolayer of MA is deposited on the surface.

Detailed Description Text - DETX (5):
The present invention uses the **ALD** process to fabricate a
metal-insulator-metal (MIM) capacitor on a semiconductor wafer, such as a
silicon wafer. It is appreciated that one problem with a prior art technique
(such as the generic CVD process) of forming capacitors on a wafer is in the
oxidation of the bottom conductive layer of the capacitor. After deposition of
the bottom conductive layer, pattern delineation (photolithographic patterning,
etching, etc.) and/or cleaning steps can oxidize the surface of the bottom
conductive layer (including, metal, metal nitride or semiconducting layer).

Detailed Description Text - DETX (6):
The extent of oxidation varies with the substrate and the cleaning process,
but typically accounts for more than 10 Angstroms. The air exposure of the
bottom conductor during pattern delineation, as well as some oxygen **plasma**
ashing processes that are conventionally applied to remove photoresist, will
oxidize the surface of the bottom electrode, which will interface with an
overlying insulator material. Parasitic oxide in the metal-dielectric

interface is undesirable, since these low quality oxides do not contribute to the insulating properties of the MIM capacitor. Worse, the added thickness may reduce the capacitance value by making the effective dielectric thicker. In addition, these poorly defined oxides may interfere with surface activation of the following dielectric **ALD** film and deteriorate the insulating properties of the **ALD** dielectric film. Furthermore, where ultrathin film layers (of 50 Angstroms or less) are being grown by **ALD,** oxidized regions of 10 Angstroms have considerable more impact than film layers (of much higher thickness) grown by conventional CVD techniques. The present invention is practiced to remove or inhibit these deficiencies.

Detailed Description Text - DETX (7):

Referring to FIGS. 1-4, one embodiment for practicing the present invention is shown. In FIG. 1, a substrate 10 (again, substrate is used herein to refer to either a base substrate or a material film layer formed on a base substrate) is shown upon which **ALD** is performed. A first conductive layer, which is typically a metal (M1) layer, 11 is deposited by **ALD**. Typically, M1 layer 11 is comprised of a metal or metal nitride, including Ta, Ta.sub.x N, Ti, TiN or Al, which is used for constructing MIM capacitors. A typical example structure for a MIM is Ta.sub.x N/Al.sub.2 O.sub.3 /Ta.sub.x N stack on HSG (high surface area polysilicon grain) layer. Thus, substrate 10 can be HSG, while M1 layer 11 can be Ta.sub.x N. With **ALD,** M1 layer 11 is deposited to an approximate thickness, of 30-50 angstroms.

Detailed Description Text - DETX (8):

Subsequently, a sacrificial layer 12 is deposited overlying layer 11 by **ALD**.

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
1	☐	☒	US 6780704 B1	20040824	29	Conformal thin films over textured capacitor electrodes	438/239	257/E21.008; 257/E21.272; 257/E21.274; 257/E21.281; 438/240; 438/761; 438/765; 438/780; 438/790	
2	☒	☒	US 6727169 B1	20040427	29	Method of making conformal lining layers for damascene metallization	438/622	438/641; 438/674	
3	☒	☒	US 6689220 B1	20040210	21	Plasma enhanced pulsed layer deposition	118/695	118/698; 118/723E; 118/723I; 118/723MW	
4	☐	☒	US 6551399 B1	20030422	19	Fully integrated process for MIM capacitors using atomic layer deposition	117/102	117/105; 117/106; 117/89	
5	☐	☒	US 6503330 B1	20030107	13	Apparatus and method to achieve continuous interface and ultrathin film during atomic layer deposition	118/715	118/723ER; 118/723IR; 118/723ME	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
1	Raaijmakers, Ivo et al.	☒	☐	☐	☐	☐	☐	☐	US 6780704	☐
2	Raaijmakers, Ivo et al.	☐	☐	☐	☐	☐	☐	☐	US 6727169	☐
3	Nguyen, Tue	☐	☐	☐	☐	☐	☐	☐	US 6689220	☐
4	Sneh, Ofer et al.	☒	☐	☐	☐	☐	☐	☐	US 6551399	☐
5	Sneh, Ofer et al.	☒	☐	☐	☐	☐	☐	☐	US 6503330	☐

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
6	☐	☒	US 6482262 B1	20021119	11	Deposition of transition metal carbides	117/84	117/88; 257/E21.171; 257/E21.584; 427/249.1; 427/249.17; 427/249.18; 427/249.19; 438/680; 438/685	
7	☐	☒	US 6475910 B1	20021105	11	Radical-assisted sequential CVD	438/685	118/715; 257/E21.17; 438/680	
8	☐	☒	US 6391785 B1	20020521	14	Method for bottomless deposition of barrier layers in integrated circuit metallization schemes	438/704	257/E21.171; 257/E21.579; 257/E21.582; 257/E21.584; 438/689	
9	☐	☒	US 6305314 B1	20011023	18	Apparatus and concept for minimizing parasitic chemical vapor deposition during atomic layer deposition	118/723R	118/723E; 257/E21.17; 257/E21.272; 257/E21.274	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
6	Elers, Kai-Erik et al.	☒	☐	☐	☐	☐	☐	☐	US 6482262	☐
7	Sneh, Ofer	☒	☐	☐	☐	☐	☐	☐	US 6475910	☐
8	Satta, Alessandra et al.	☒	☐	☐	☐	☐	☐	☐	US 6391785	☐
9	Sneh, Ofer et al.	☒	☐	☐	☐	☐	☐	☐	US 6305314	☐

	U	1 [1]	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
10	☐	☒	US 6200893 B1	20010313	11	Radical-assisted sequential CVD	438/685	117/92; 117/93; 257/E21.17; 427/255.394; 427/576; 427/578; 427/96.8; 438/677; 438/680	

	Inventor	S	C	P	2	3	4	5	Image Doc. Displayed	PT
10	Sneh, Ofer	☒	☐	☐	☐	☐	☐	☐	US 6200893	☐